II. AMENDMENTS TO THE CLAIMS

The following listing of claims replaces all prior versions, and listings, of claims in the application:

1. (Currently amended) A method of forming a gas dielectric structure for a semiconductor structure, the method comprising the steps of:

forming an opening for semiconductor structure in a dielectric layer on a substrate, wherein the opening includes both a wiring opening and a via opening, wherein the via provides a vertical connection to an interconnect line;

depositing a sacrificial layer over the opening such that the sacrificial layer fails to substantially fill the opening;

performing a directional etch on the sacrificial layer to form a sacrificial layer sidewall on the opening after depositing the sacrificial layer;

depositing a conductive liner over the opening after performing the directional etch;

depositing a metal in the opening after depositing the conductive liner to form a wire and a contact via;

planarizing the metal and the conductive liner after depositing the metal;

removing the sacrificial layer sidewall <u>using a dry etching process,</u> after the metal and the conductive liner are planarized, forming a void, wherein the void extends along a side of the contact via and the wire; and

depositing a cap layer over the void to form the gas dielectric structure.

2-3. (Cancelled)

4. (Original) The method of claim 1, wherein the forming step includes performing a dual damascene process.

5. (Original) The method of claim 1, wherein the forming step includes depositing a hard mask, patterning the hard mask and etching the hard mask.

6. (Original) The method of claim 1, further comprising the step of depositing a non-conductive liner prior to the step of depositing the sacrificial layer.

7. (Original) The method of claim 1, wherein the conductive liner includes at least one of the group consisting of: tantalum (Ta), tantalum nitride (TaN), titanium (Ti), titanium nitride (TiN), tungsten (W) and niobium (Nb).

8. (Previously presented) The method of claim 1, wherein the sacrificial layer includes one of the group consisting of: aluminum (Al) and silicon dioxide (SiO_2).

9-10. (Cancelled)

11. (Currently amended) A method of forming a gas dielectric structure for a semiconductor structure, the method comprising the steps of:

performing a dual damascene process to form an opening including both a wiring

opening and a via opening in a dielectric layer on a substrate, wherein the via provides a vertical connection to an interconnect line;

depositing a sacrificial layer over the opening;

performing a directional etch on the sacrificial layer to form a sacrificial layer sidewall wherein the directional etching removes the sacrificial layer only from substantially horizontal surfaces;

depositing a conductive liner over the opening after performing the directional etch;

depositing a metal in the opening after depositing the conductive liner to form a wire and a contact via;

planarizing the metal and the conductive liner after depositing the metal;

removing the sacrificial layer sidewall using a dry etching process, after the metal and the conductive liner are planarized, forming a void, wherein the void extends along a side of the contact via; and

depositing a cap layer over the void to form the gas dielectric structure.

12. (Cancelled)

13. (Original) The method of claim 11, wherein the forming step includes depositing a hard mask, patterning the hard mask and etching the hard mask.

14. (Original) The method of claim 11, further comprising the step of depositing a non-conductive liner prior to the step of depositing the sacrificial layer, wherein the non-

conductive liner includes one of the group consisting of: silicon nitride (Si_3N_4) and silicon dioxide (SiO_2).

15. (Original) The method of claim 11, wherein the conductive liner includes at least one of the group consisting of: tantalum (Ta), tantalum nitride (TaN), titanium (Ti), titanium nitride (TiN), tungsten (W) and niobium (Nb).

16. (Previously presented) The method of claim 11, wherein the sacrificial layer includes one of the group consisting of: aluminum (Al) and silicon dioxide (SiO_2).

17. (Currently amended) A method of forming a gas dielectric structure for a semiconductor structure, the method comprising the steps of:

performing a via-first dual damascene process to form an opening including both a wiring opening and a via opening in a dielectric layer on a substrate, wherein the via provides a vertical connection between to an interconnect line;

depositing a sacrificial layer over the opening such that the sacrificial layer fails to substantially fill the opening;

performing a directional etch on the sacrificial layer to form a sacrificial layer sidewall, wherein the directional etching removes the sacrificial layer only from substantially horizontal surfaces;

depositing a conductive liner over the opening after performing the directional etch;

depositing a metal in the opening after depositing the conductive liner to form a

wire and a contact via;

planarizing the metal and the conductive liner after depositing the metal;

removing the sacrificial layer sidewall using a dry etching process, after the metal and conductive liner are planarized, forming a void that extends along a side of the contact via; and

depositing a cap layer over the void to form the gas dielectric structure.

18. (Original) The method of claim 17, further comprising the step of depositing a non-conductive liner prior to the step of depositing the sacrificial layer, wherein the non-conductive liner includes one of the group consisting of: silicon nitride (Si_3N_4) and silicon dioxide (SiO_2).

19. (Original) The method of claim 17, wherein the conductive liner includes one of the group consisting of: tantalum (Ta), tantalum nitride (TaN), titanium (Ti), titantium nitride (TiN), tungsten (W) and niobium (Nb).

20. (Previously presented) The method of claim 17, wherein the sacrificial layer includes one of the group consisting of: aluminum (Al) and silicon dioxide (SiO_2).